REMARKS

In the Office Action dated September 22, 2004, the Examiner has finally rejected claims 1-65 pending in the application on the basis of new grounds of rejection and newly cited art. Applicant respectfully requests reconsideration and withdrawal of the finality of the rejection of the Office Action dated September 22, 2004.

A good and sufficient reason why the present response is necessary and was not earlier presented is that entirely new references have been cited in the present final rejection dated September 22, 2004 (37 §CFR 1.116 (c)). The new references are U.S. Patent Number 5,521,639 to Tomura, et al. ("Tomura"), Japanese Patent Number JP02000004403A to Hiyama, et al. ("Hiyama"), and U.S. Patent Number 6,275,191 to Lesea, et al. ("Lesea"), which are for the first time brought to Applicant's attention by means of the present final rejection dated September 22, 2004. The new references, i.e., Tomura, Hiyama, and Lesea, were not cited in the present application prior to the instant final rejection. Since Tomura, Hiyama, and Lesea are references upon which the Examiner has now relied, Applicant believes that it would be manifestly unfair for the Patent Office not to consider Applicant's arguments which are necessitated due to the newly cited references, Tomura, Hiyama, and Lesea. As such, a good and sufficient reason exists, as required by 37 CFR §1.116(c), for considering Applicant's present response and withdrawing the finality of the present Office Action.

A. Rejections of Claims 1-4, 8-10, 12, 13, 15-18, 22-24, 26, 27, 29-40, 45-48, 50-59, and 65 under 35 USC §103(a)

The Examiner has rejected claims 1-4, 8-10, 12, 13, 15-18, 22-24, 26, 27, 29-40, 45-48, 50-59, and 65 under 35 USC §103(a) as being unpatentable over U.S. Patent Application

Number 6,396,539 B1 to Heller, et al. ("Heller"), in view of Tomura, and Hiyama. For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by independent claims 1, 29, 37, 45, 51, and 57, is patentably distinguishable over Heller.

Embodiments according to the present invention address a need in the art for an improved process and system for storing addresses of defective pixels in an imaging device for subsequent retrieval. Present embodiments relate to a permanently programmable solid-state device. One time programmable ("OTP") device 100 includes driver circuit 104 that drives programmable memory unit 102. Driver circuit 104 includes a plurality of logic inverters that drive the terminals of the MOSFETs in programmable memory unit 102, and a number of high-voltage drivers (e.g., amplifiers) that drive the gates of the MOSFETs in the programmable memory unit 102. When programmable memory unit 102 is encoded, the drivers drive the voltage levels into the MOSFETs to predetermined values based on whether a logic state 1 or logic state 0 is to be represented in the MOSFET. OTP device 100 further includes access circuit 106. Access circuit 106 has a number of amplifiers that output a logic state 1 or logic state 0 from a given MOSFET corresponding to the state of breakdown or intactness of the gate oxide of that MOSFET.

Driver circuit 104 is separate from access circuit 106 as described herein and as shown in Figures 1 and 5. Furthermore, driver circuit 104 and access circuit 106 fulfill different functions from each other. Driver circuit 104 is used for writing to programmable memory unit 102. Driver circuit 104 programs the programmable memory unit with addresses of defective pixels by programming memory cells within the programmable memory unit with a first logic value or a second logic value. The first logic value represents a good (i.e. non-defective) pixel at the corresponding location (e.g. address). The second logic value represents a defective pixel at the corresponding location. The individual memory cells are associated with respective pixel

locations. Referring to Figure 8 and the corresponding written description, driver circuit 104 functions to drive an inverter to ground corresponding to a row of the memory cells that are to be programmed.

On the other hand, access circuit 106 is used for accessing programmable memory unit 102 and is used for identifying addresses of defective pixels. Referring to Figure 8 and the corresponding written description, access circuit 106 drives a row of the memory cells to ground that are to be read out. Independent claims 1, 29, 37, 45, 51, and 57 recite various features related driver circuit 104 and/or access circuit 106 as discussed herein.

In contrast to the present invention as defined by amended independent claims 1, 29, 37, 45, 51, and 57, Heller discloses single controller unit 16 including analog-to-digital circuitry. See, for example, Heller at column 3, line 57 and Figure 2. Heller teaches that the operation of system 100 is orchestrated by system controller 122. System controller 122 is connected to communication interface 124. See, for example, Figure 1 of Heller.

The Examiner seems to be asserting that Heller teaches separate driver circuit 104 and access circuit 106 within controller unit 16. However, Applicants respectfully submit that the Examiner has not pointed to any such teaching in Heller. Heller discusses controller unit 16 as a single unit and does not specify driver circuit 104 and access circuit 106. Without such teaching in a single reference or in a combination of references, the rejection should be withdrawn. Heller does not teach driver circuit 104 for writing to programmable memory unit 102, and separate access circuit 106 for accessing programmable memory unit 102 and for identifying addresses of defective pixels. Additionally, Heller does not disclose, teach, or even suggest an access circuit configured to drive a row of the memory cells to ground that are to be read out.

Heller does not disclose, teach, or suggest the elements of independent claims 1, 29, 37, 45, 51, and 57. Furthermore, there is no teaching or suggestion to combine Heller with other art of record. Therefore, Heller, singly or in combination with other art of record, does not disclose, teach or suggest the present invention as defined by independent claims 1, 29, 37, 45, 51, and 57.

Furthermore, Tomura does not cure the deficiencies of Heller. Tomura is directed to a solid-state imaging apparatus for producing an image signal. The apparatus described in Tomura has an active pixel region comprised of a plurality of active light receiving pixels, and an optical black region disposed at the peripheral portion of the active pixel region, with a reference pixel in the optical black region. However, as the Examiner acknowledges, Heller and Tomura fail to teach that an access circuit is configured to drive a row of the memory cells to ground that are to be read out. Further, Tomura does not teach a separate access circuit and driver circuit.

Tomura does not disclose, teach, or suggest the elements of independent claims 1, 29, 37, 45, 51, and 57. Furthermore, there is no teaching or suggestion to combine Tomura with other art of record. Therefore, Tomura, singly or in combination with other art of record, does not disclose, teach or suggest the present invention as defined by independent claims 1, 29, 37, 45, 51, and 57.

In addition, Hiyama does not cure the deficiencies of Heller and Tomura. Hiyama is directed to a photoelectric converter. The photoelectric converter comprises photoelectric conversion element 1, memory means 4 that stores a photoelectric conversion signal of photoelectric conversion element 1, read means 5 that reads the photoelectric conversion signal, and switch means that transfers the photoelectric conversion signal to memory means 4. Hiyama teaches resetting the memory means 4 before and after reading the photoelectric signal.

In contrast, for example, independent claim 1 of the present application recites "an access circuit that enables access to the programmable memory unit, wherein the access circuit is configured to drive a row of the memory cells to ground that are to be read out." Referring to the present application, on page 18, access circuit 106 generally accesses and reads data one row at a time. For example, when a particular row is to be read out by access circuit 106, the row driver 406 associated with that row 412 drives row 412 to ground, while the other row drivers and all of the column drivers are tristated. This technique and circuitry is different than that of the simple memory reset of Hiyama.

Hiyama does not disclose, teach, or suggest the elements of independent claims 1, 29, 37, 45, 51, and 57. Furthermore, there is no teaching or suggestion to combine Hiyama with other art of record. Therefore, Hiyama, singly or in combination with other art of record, does not disclose, teach or suggest the present invention as defined by independent claims 1, 29, 37, 45, 51, and 57.

For the foregoing reasons, Applicant respectfully submits that the present invention as defined by independent claims 1, 29, 37, 45, 51, and 57 is not taught, disclosed, or suggested by the art of record. Thus, independent claims 1, 29, 37, 45, 51, and 57 are patentably distinguishable over the art of record. As such, the claims depending from independent claims 1, 29, 37, 45, 51, and 57 are, *a fortiori*, also patentable for at least the reasons presented above and also for additional limitations contained in each dependent claim.

B. Rejections of Claims 5-7, 11, 14, 19-21, 25, 28, 41-44, 49, and 60-64 under 35 USC §103(a)

The Examiner has rejected claims 11, 25, and 49 under 35 USC §103(a) as being unpatentable over Heller, in view of Tomura, Hiyama, and U.S. Patent Number 6,141,453 to Banham, et al. ("Banham"). The Examiner has rejected claims 5-7 and 19-21 under 35 USC §103(a) as being unpatentable over Heller, in view of Tomura, Hiyama, and U.S. Patent Application Number US 2002/0001219 A1 to Forbes, et al. ("Forbes"). The Examiner has rejected claims 14, 28, 41, and 42 under 35 USC §103(a) as being unpatentable over Heller, in view of Tomura, Hiyama, and U.S. Patent Number 6,532,514 B1 to Haroun, et al. ("Haroun"). The Examiner has rejected claims 43 and 44 under 35 USC §103(a) as being unpatentable over Heller, in view of Tomura, Hiyama, Haroun, and U.S. Patent Number 5,410,511 to Michiyama ("Michiyama"). The Examiner has rejected claims 60-64 under 35 USC §103(a) as being unpatentable over Heller, in view of Tomura, Hiyama, and U.S. Patent Number 6,275,191 to Lesea, at al. ("Lesea").

Applicant respectfully submits that claims 5-7, 11, 14, 19-21, 25, 28, 41-44, and 49 depend from independent claims 1, 29, 37, 45, 51, and 57, and thus, claims 5-7, 11, 14, 19-21, 25, 28, 41-44, and 49 should be allowed at least for the same reasons discussed above in conjunction with patentability of the independent claims.

C. Conclusion

Based on the foregoing reasons, an early notice of allowance for claims 1-65 remaining in the present application is respectfully requested.

Respectfully Submitted,
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